METRRA REPAIR FINAL REPORT

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CONTRACT DAA70-77-C-0184

SUBMITTED TO

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ARIZONA DIVISION • • • LITCHFIELD PARK, ARIZONA

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ABSTRACT

This report describes a 13-month program of improvement, repair, and checkout of a Synthetic Aperture Metal Reradiation Reconnaissance Radar System (METRRA/SAR) for the U.S. Army Mobility Equipment Research, Ft. Belvoir, under Contract DAA70-77-C-0184. The purpose of the system is to detect tactical targets by sensing reradiated third harmonic signals produced by rectification of transmitted pulses at metal-to-metal junctions in the targets. Detection and location are enhanced by synthetic aperture processing of third harmonic signals. The equipment items improved were the transmitter, processor, and scan converter subsystems. The improvements and repairs made were those indicated during flight tests, on a previous contract, which would enhance the performance and reliability of the system. The report details the improvements and repairs made and their effect on system operation.

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SECTION I — INTRODUCTION

1. GENERAL

This document is a final report on U.S. Army Mobility Equipment Research Contract DAA70-77-C-0184 for improvement of the airborne METRRA/SAR system. The contractual effort beginning 31 August 1977 and ending 30 September 1978 concerned itself with certain items of improvement indicated during system flight tests conducted under contract DAAG53-75-C-0177.

2. OPERATION

The METRRA system takes advantage of third harmonic reradiation properties of imperfectly contacting conductors which exhibit a "diode" effect, thereby allowing it to discriminate between metallic and nonmetallic objects.[a]

The system, configured as shown in Figure 1, consists of one fundamental frequency transmitter, two coherent receivers, a real-time synthetic aperture processor, and a scan converter display. Objects are illuminated by a pulse transmitted at the fundamental frequency, and fundamental returns are received for all objects as with conventional radars. Those objects having harmonic reradiation properties radiate detectable quantities of the target-generated third harmonic frequency as well as fundamental returns. Using two receivers, one tuned to the fundamental and the other to the third harmonic frequency, the system discriminates between those objects that provide third harmonics and those that do not.

3. GENERAL REQUIREMENTS

The contract statement of work specifies certain functional and hardware improvements to be performed on the transmitter, processor, and scan converter subsystems. While hardware improvements were well defined, other functional improvements were specified by defining a change in various aspects of subsystem operation. How these functional changes were accomplished is discussed in detail in Section II. After completion of all improvements, the subsystems were laboratory tested to verify performance to specifications, and the individual improvements were tested per METRRA Repair Test Plan submitted 12 September 1978 (see Appendix A).

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[a]Harger, R.O.: "Harmonic Radar Systems for Near-Ground In-Foliage Nonlinear Scatterers," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-12, No. 2, March 1976.

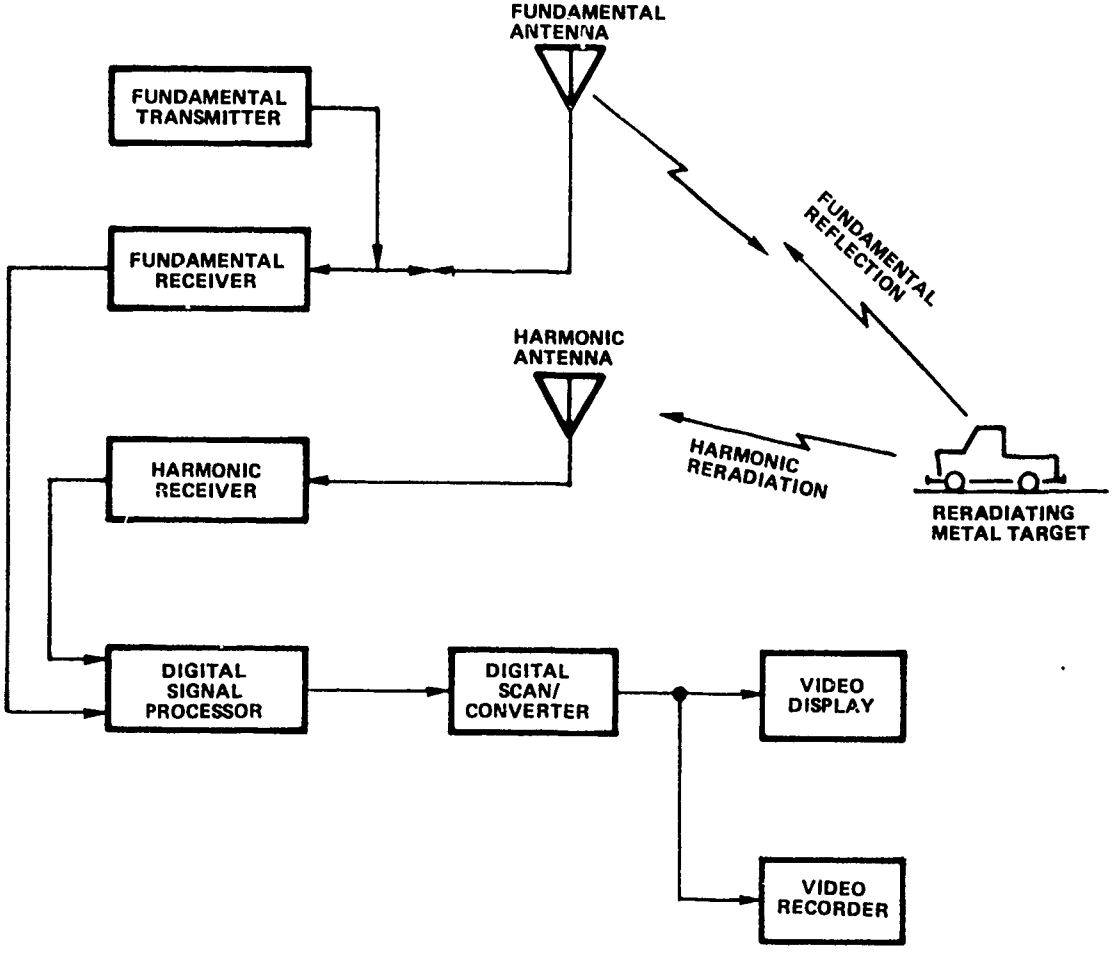

Figure 1 — METRRA System Block Diagram

4. RESULTS

Performance of the subsystems complied with their respective specifications when tested using built-in test features combined with external test measurements where possible. The subsystem improvements incorporated under this contract were tested per the METRRA Repair Test Plan, thereby demonstrating compliance with the functional requirements indicated in the contract statement of work.

SECTION II — DESCRIPTION OF IMPROVEMENTS

1. GENERAL

The contract statement of work indicated certain improvements to be performed on the three METRRA/SAR subsystems. Each improvement is listed here followed by the actions taken and the details of the individual implementations.

2. DETAILED DESCRIPTION

a. Improve METRRA Subsystem Performance

Improve METRRA subsystem performance by redesigning the cooling system, replacing power supplies, and replacing analog-to-digital converters (ADC) with high-speed, low-drift models.

(1) Transmitter Subsystem

Certain improvements to the transmitter subsystem were indicated during the METRRA flight test program. Poor reliability of both the high- and low-voltage supplies coupled with extended repair cycles and limited documentation prompted replacement of sections of the main supply unit with separate modular units at that time. Excessive operating temperatures of the transmitter output stages were also noted as a source of difficulty. Continued intermittent failures of the transmitter main supply unit resulted in the requirement to replace it and improve transmitter cooling under this contract. A modular concept was used in replacing the existing supply unit which facilitates maintenance in the event of failure. The supply was replaced by separate units for each voltage and each transmitter stage as follows:

Quantity	Capacity
5	7 kV, 250 W
1	3.5 kV, 250 W
2	–100 VDC, 200 MA
1	30 VDC, 1 A
1	115 V, 400 Hz, 800 VA

In addition to the above supplies, three filament transformers were installed to provide 5 VAC, 15 A and 6.3 VAC, 3 A filament power to the amplifier and driver stages. The supplies were located near their respective loads within the transmitter subchassis. The modular

approach simplified transmitter wiring such that it became both practical and advantageous to install new harnessing, control circuits, and load protection circuits in the transmitter. All existing wiring was removed from the transmitter and replaced with new cabling. Unused wiring in the receiver subchassis was removed. High-voltage supplies were installed in the transmitter chassis adjacent to their respective tube stages. The five tube stages and their respective supplies were incorporated into one common heat sink and a forced air cooling system was supplied by high-volume cooling fans (see Figure 2). Air flow within the receiver chassis was also increased with the installation of a higher volume fan.

In addition to satisfying contract requirements, repairs were made as indicated during adjustment and checkout. Amplifier tubes in the transmitter output stages were replaced. Coupling capacitors in the driver and output stages were replaced with new low-inductance units. This combination of transmitter repairs thus resulted in substantial increases in efficiency and power output as compared to measurements taken during the previous flight test contract. Transmitter output characteristics and typical output pulses are shown in Figure 3.

(2) Processor Subassembly

The major improvement made to the METRRA processor subassembly, excluding subchassis changes to be discussed in paragraph 2.b., was replacing the ADCs. The original units exhibited poor temperature stability and sampling characteristics. ADCs with the desired sample rate (10 to 15 MHz) and bandwidth have only recently become commercially available. Although several ADCs are now available in this frequency range, only one of these provided adequate temperature stability. Operational prototypes of this unit had been built and tested by the manufacturer, and availability and lead time for production units was quoted within the time frame of the contract. However, extended production delays compelled procurement of an alternate choice which required additional hardware designed to compensate for inadequate temperature offset characteristics.

Each of the three ADC assemblies consists of two printed circuit cards. The ADC card holds the ADC integrated circuit, input buffer, and regulators; and the offset correction card holds the offset correction circuits and output drivers. The ADC card is provided as an assembly from the manufacturer (TRW TDC 1007 PCB). Figure 4 is a block diagram of the ADC assembly. A relay at the input to the ADC selects the receiver video when the transmitter is radiating (ON) and a source termination when the transmitter is in STANDBY. With the

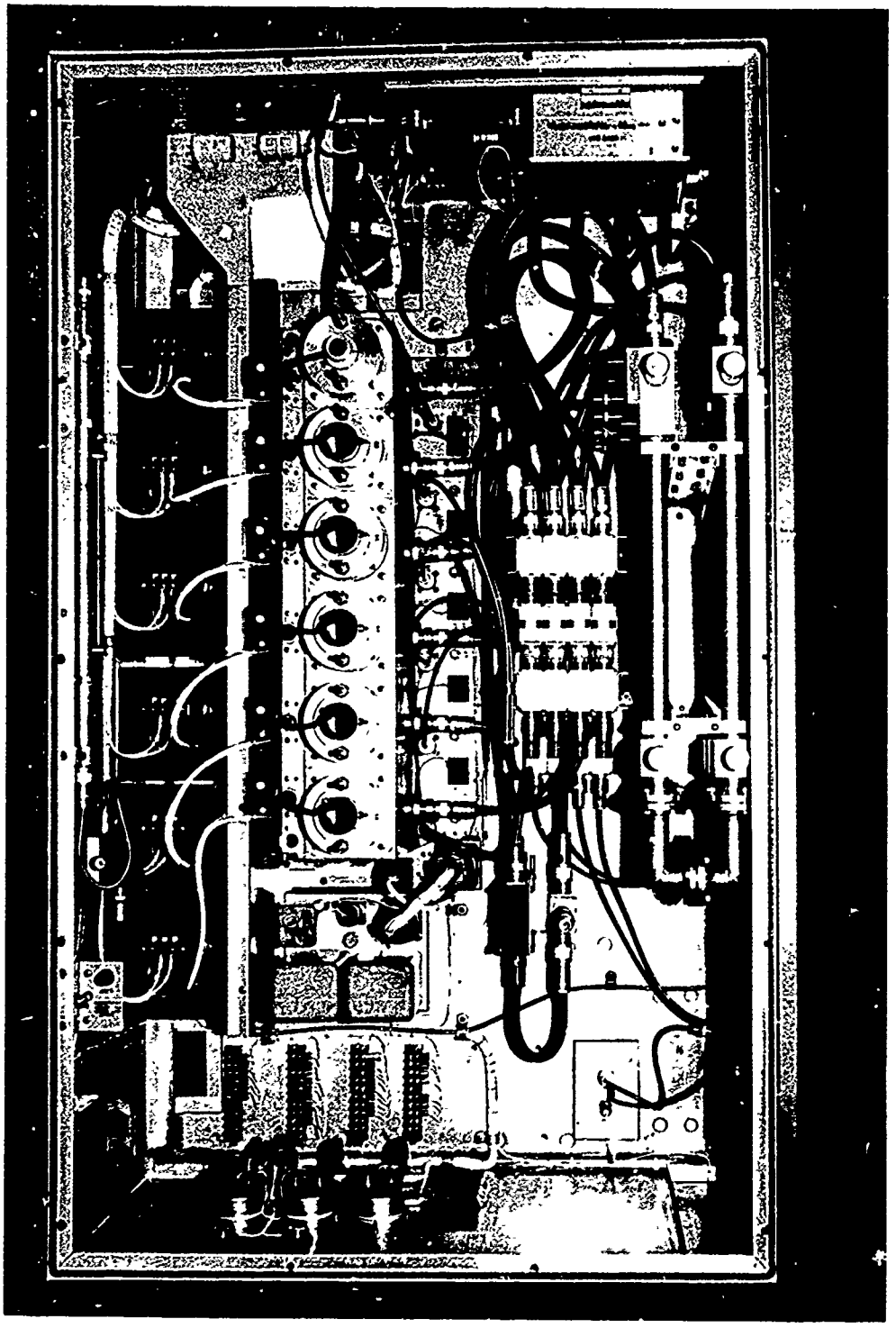

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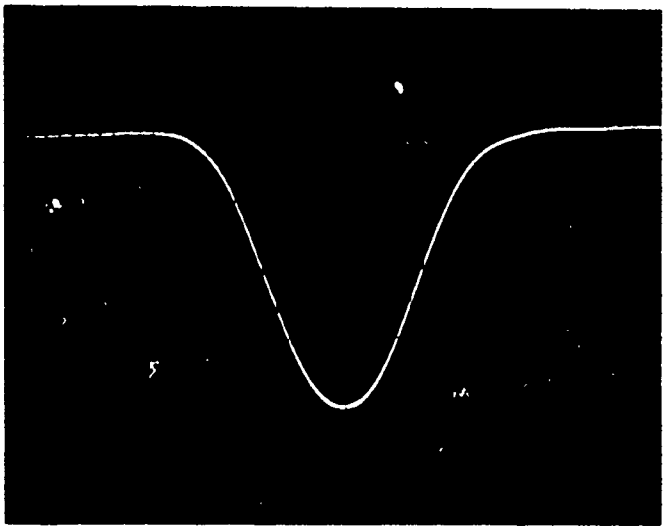
Figure 2 — Transmitter Chassis

Output Stage	Output dBM	Output kW	Pulse Width (ns)
1	+76.8	48	120
2	+76.5	45	120
3	+77.0	50	120
4	+76.4	44	120



Typical Detected Output Pulse

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Figure 3 — Transmitter Output Characteristics

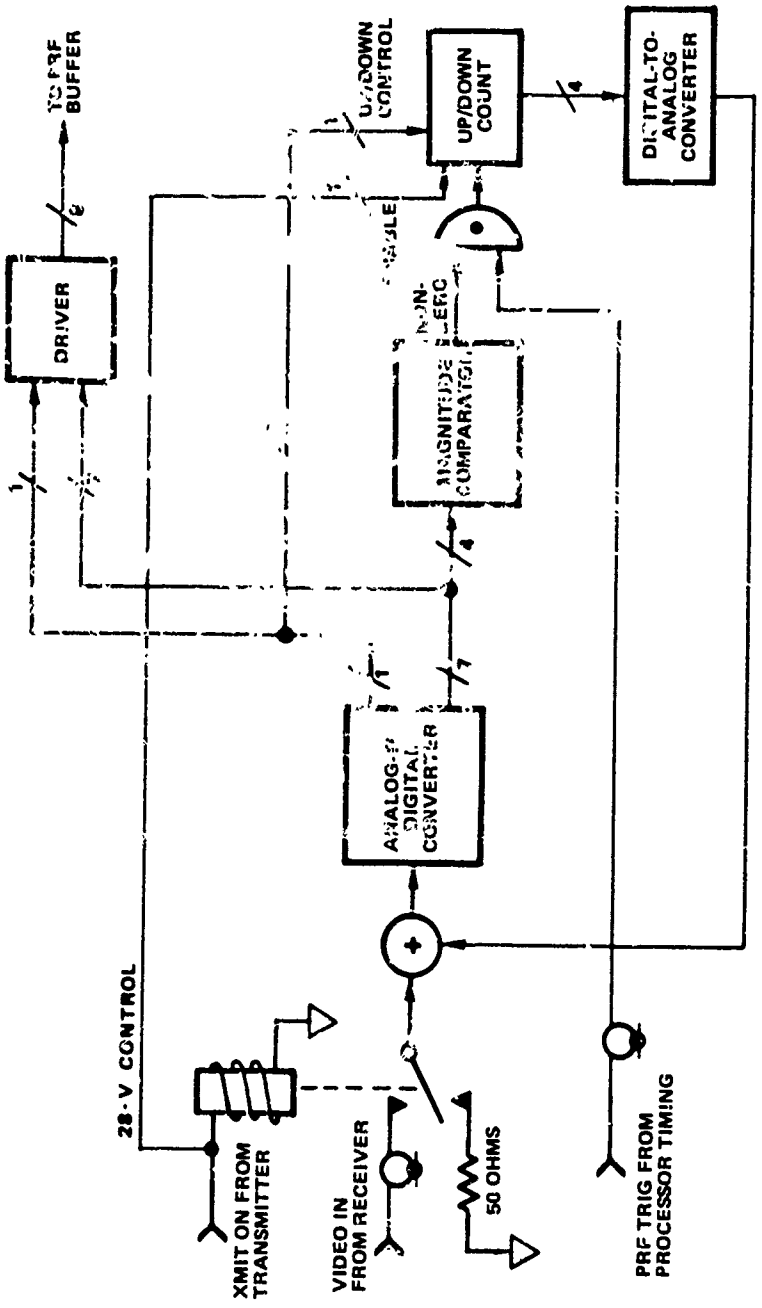


Figure 4 — ADC Assembly Block Diagram

transmitter in STANDBY the offset correction circuits are enabled and zero input is applied to the ADC. The ADC output is magnitude compared to zero and enables the UP/DOWN counter clock if greater or less than zero. The sign bit determines the direction of count. The counter clock is available once per PRF. The count value is converted to a voltage by the digital-to-analog converter (DAC) whose magnitude is equivalent to one-half a least significant bit (LSB) of the ADC multiplied by the counter value. The DAC output magnitude increases one-half LSB per PRF until the output offset falls between ±1 LSB. At this time the ADC output is zero and the count clock is disabled by the magnitude comparator. When the transmitter is set to ON, the counter is disabled providing a constant offset correction during video conversion. This configuration provides both long- and short-term stability.

b. Improve Display Characteristics

(1) Redesign Range Data Fill-in Function

The range data fill-in (sin X/X range weighting) was initially designed to reduce target sidelobes. Because of the nature of METRRA target returns and the capabilities of the processor limit and roundoff functions, strong METRRA returns were often saturated in the processor prior to data fill-in. When displayed on the monitor, such targets could be manipulated with the scan converter offset and gain controls to appear as multiple targets in range. Targets one and two range cells wide, whose peak amplitudes were normalized to a maximum in the processor limit and roundoff function, would appear after range data fill-in as shown in Figures 5(A) and 5(B), respectively. If the targets were expanded in the scan converter such that the video output was confined within the dotted lines, a single target would appear on the display as up to three targets in range. The weighting of the range data fill-in function was changed to a linear weighting to produce processor outputs as shown in Figures 5(C) and 5(D). This weighting increases first sidelobe amplitudes slightly but eliminates multiple target displays independent of scan converter control settings.

(2) Provide Calibrated Processor Controls

The processor NEAR RANGE control is selectable in one-tenth kilometer increments from 0.1 to 9.9 kilometers. Range time is measured by counting a 10-MHz clock phased with the PRF.

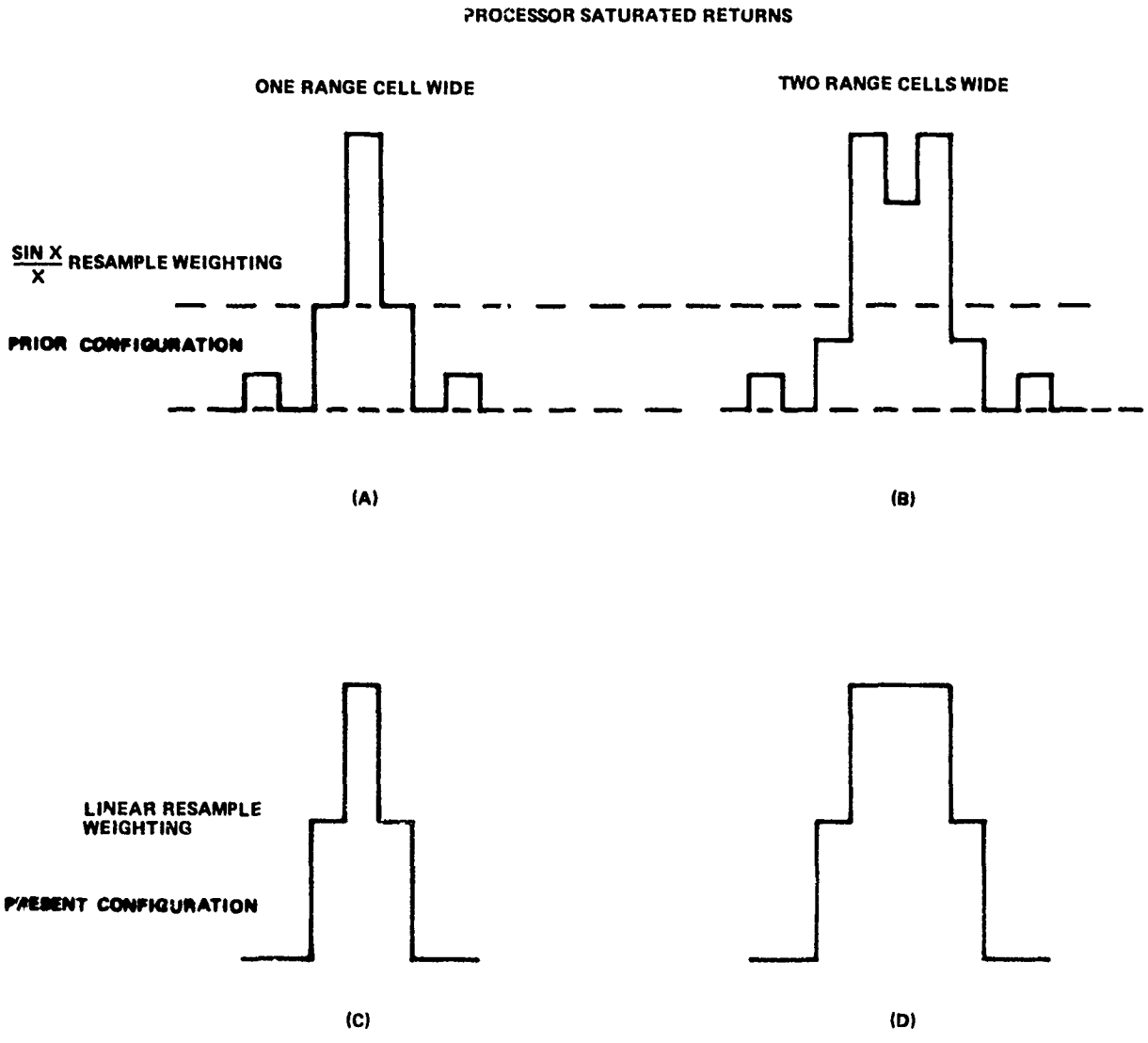


Figure 5 — Range Data Fill-in Weighting

The desired time increment for 0.1-kilometer range increments is

$$T = \frac{2R}{C} = \frac{(2)(100)\ \text{meters}}{3 \times 10^8\ \text{meters/s}} = 660\ \text{ns} \quad .$$

Using a 10-MHz clock, six clock periods per one-tenth kilometer provides a 10-percent error in near range determination. Increasing or decreasing the 10-MHz clock would provide a clock period which is an even submultiple of the range time increment of 660 ns. This would provide accurate range timing coinciding with the range control. The 10-MHz clock referred to is the ADC sampling clock. The clock may not be reduced in frequency because of range bandwidth considerations. The required range interval (660 ns) may be obtained using seven clock periods of 10.6 MHz

$$T = \frac{7}{10.6\ \text{MHz}} = 660\ \text{ns} \quad .$$

In the original design, the range error was tolerated because the ADC used had a maximum sample rate of 10 MHz. The ADCs have been replaced under this contract with units whose maximum sample rate is far in excess of 10 MHz. An adjustment in frequency of the sample clock to 10.6 MHz provides calibrated 0.1-kilometer increments in range.

(3) Near/Far Range Cross Talk

Examination of the processor, scan converter, and display subsystems indicated no cross talk between near and far range or between channels with one exception. A residue from an azimuth line of data appeared in the first few near range cells of the next line of the processor output. This occurred in the data fill-in circuits where each line of data was operated on serially and where several consecutive range cells were stored. Therefore, the last two range cells of any azimuth line were combined by the data fill-in function with the first two cells of the succeeding line. This effect was defeated by clearing the holding registers in the data fill-in circuits between each line of azimuth data.

(4) Modify Processor to Provide a Constant Aspect Display (One-to-One Display Aspect Ratio)

Several possibilities were examined to satisfy this requirement. Two possible solutions could have been implemented without major hardware changes to the existing system. One possible solution was to extend the existing display format algorithm by expanding the azimuth

data within the scan converter by factors of two between designated ranges of the NEAR RANGE control. This, combined with varying the data rate of the scan converter output (varying the display width of the range data), would provide a square aspect display. By this method the display would become narrower in range as the NEAR RANGE control was increased until the range display decreased to one-half the full display width. With further increase of the NEAR RANGE control the azimuth data would be expanded by a factor of two in the memory, and the range data would again occupy the full display. This approach, although easy to implement from the existing scan converter, provides less than a desirable range scale for certain near range settings. For these range settings the constant full range swath of 1.36 kilometers is presented over one-half the horizontal width of the screen making distinction between adjacent targets in range difficult. For this reason a second approach was implemented which, although requiring additional logic and storage, provided for data to fill the display screen independent of processor range settings. The approach used bypasses the existing display format logic and resamples the azimuth data as a function of near range, prior to loading into the display refresh memory. In so doing the distance in meters per azimuth display line is held constant such that the azimuth and range scales on the display are equal.

Figure 6 is a block diagram showing the basic operation of the azimuth resampler for either the fundamental or harmonic channel. The resampler accepts data upon demand of the processor and provides resampled data between adjacent azimuth lines at constant distance intervals of aircraft travel (8.4- and 16.8-meter intervals for harmonic and fundamental, respectively). The distance intervals are determined from the system range swath and the geometry of a standard 525-line television monitor. The resample interval is obtained by integrating the aircraft velocity, scaled to overflow at the prescribed distance. The number of new azimuth lines generated between any two processor azimuth lines is the ratio of the processor aperture to the fixed resample distance. Weighting of adjacent azimuth lines to generate a new line is accomplished by dividing the time between processor data lines into 16 equal intervals. When a resample is initiated, its location in time with respect to the two stored processor azimuth lines is known and used to linearly weight the stored data to generate the resampled line. At the command of the velocity integrator a resample is initiated which provides an output data sync followed by 192 resampled range cells. If the processor is actively

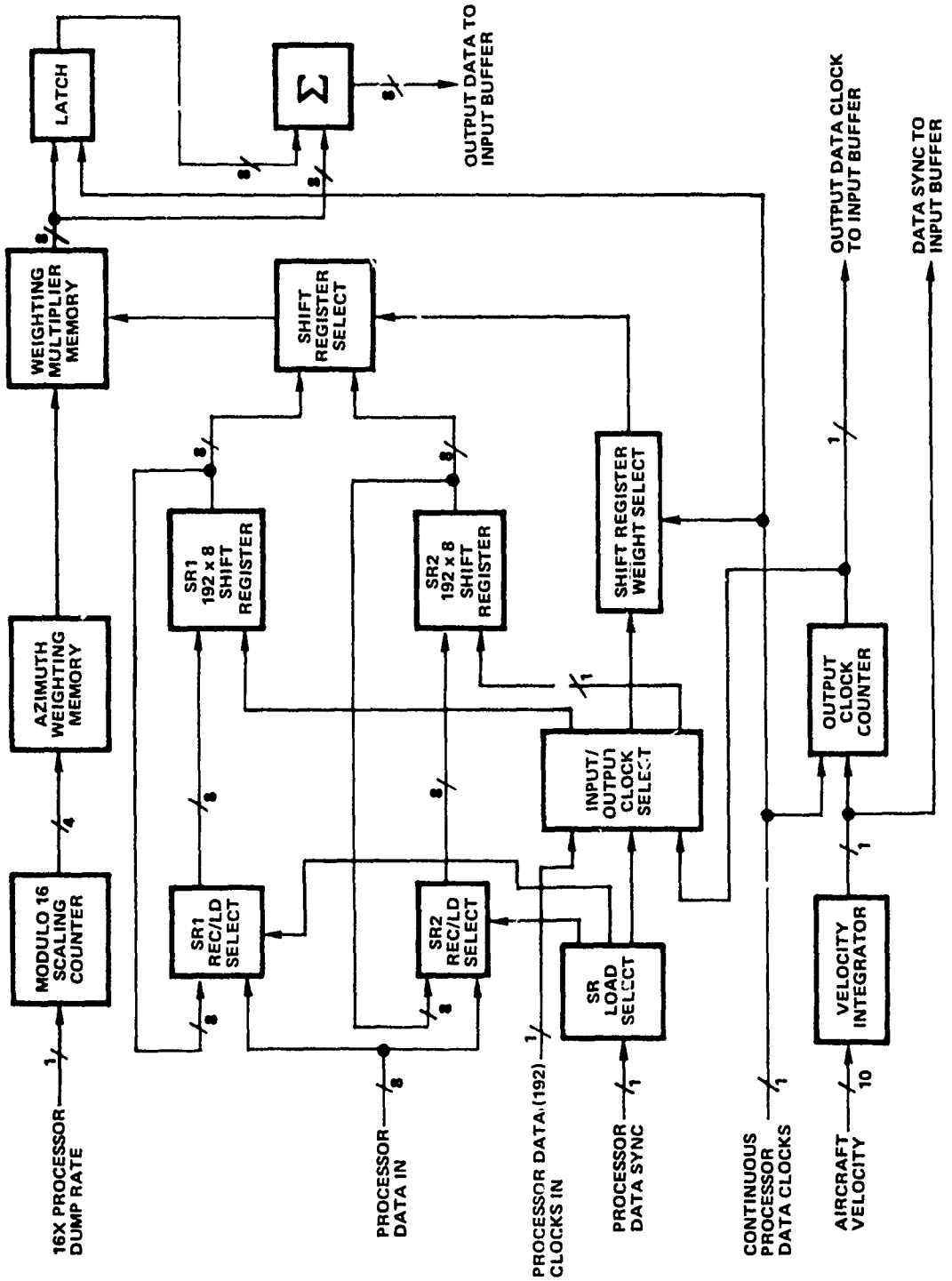


Figure 6 — Azimuth Resampler Block Diagram

loading SR1 or SR2, the resample is inhibited until the processor load is complete. Resampling is accomplished by linearly weighting like range cells of the adjacent azimuth lines stored in SR1 and SR2 and summing the results to obtain a new range cell. This operation is performed for each of the 192 range cells stored in SR1 and SR2.

APPENDIX A –

AIRBORNE METRRA REPAIR TEST PLAN

(AAP-47444)

GAA-131

GOODYEAR AEROSPACE

CORPORATION

ARIZONA DIVISION

LITCHFIELD PARK, ARIZONA 85340

AIRBORNE METRRA REPAIR TEST PLAN

Contract No. DAAK70-77-C-0184

Goodyear Aerospace Arizona Division

Litchfield Park, Arizona 85340

AAP-47444

Code 99696

12 September 1978

I. GENERAL

The purpose of the following tests is to verify that the system improvements, as outlined in the contract statement of work, have been effectively implemented. Improvements were performed on the transmitter, processor and scan converter sub-systems. Tests will be performed on a subsystem level. Subsystems other than the subject subsystem will be used as testing aids to provide test inputs or demonstrate test results as required.

II. DESCRIPTION OF TEST

A. Transmitter

1. Improved Transmitter Cooling:

Transmitter cooling was enhanced by increasing airflow through existing ducting with the installation of high volume fans. Since the transmitter does not contain any thermal sensing circuits there is no demonstrative procedure to verify repairs to the cooling system other than note the difference in the old and present fan airflow capabilities.

2. Replace Transmitter Power Supplies:

Transmitter power supply performance may be verified by examining transmitted outputs for proper power, phase and pulse width of each output stage.

a. Procedure

_____ Step 1. Connect transmitter as per test configuration of Figure 1.

_____ Step 2. Turn transmitter on as follows and allow 2 minutes for temperature stabilization.

a. Install proper RF loads on outputs

b. Local/Remote switch to "Local"

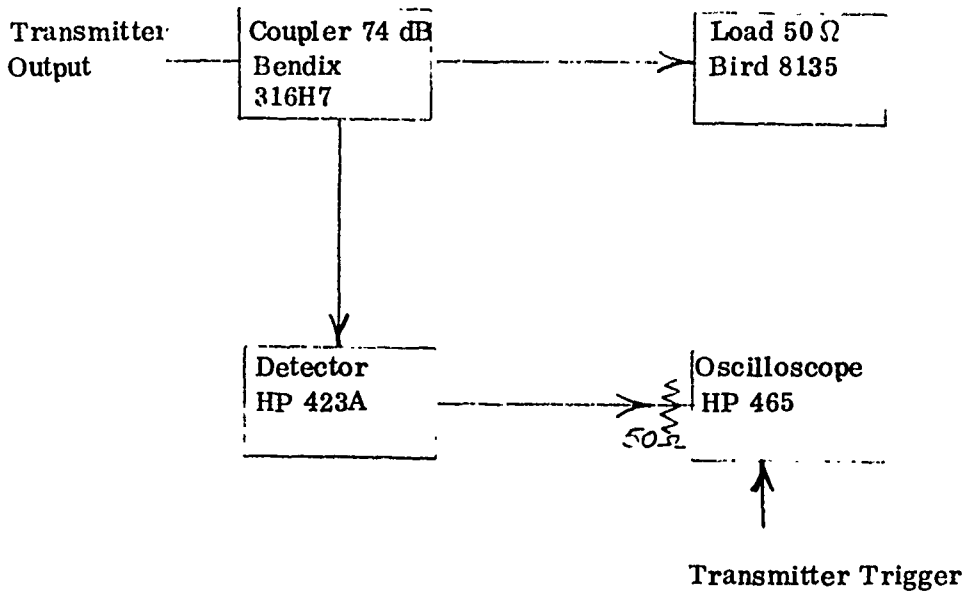
c. System switch to "On"

d. Wait for transmitter ready light

e. Transmitter switch to "On"

_____ Step 3. Measure power and pulse width of each stage and record.

_____ Step 4. Connect transmitter as per test configuration of Figure 2.



NOTES:

1. Detector calibrated for power input of 0 dBM to +4 dBM versus voltage output into 50 Ω load.

2. Unused transmiter outputs terminated into 50 Ω load (Bird 8135).

Figure (1) - Transmitter output and pulse width.

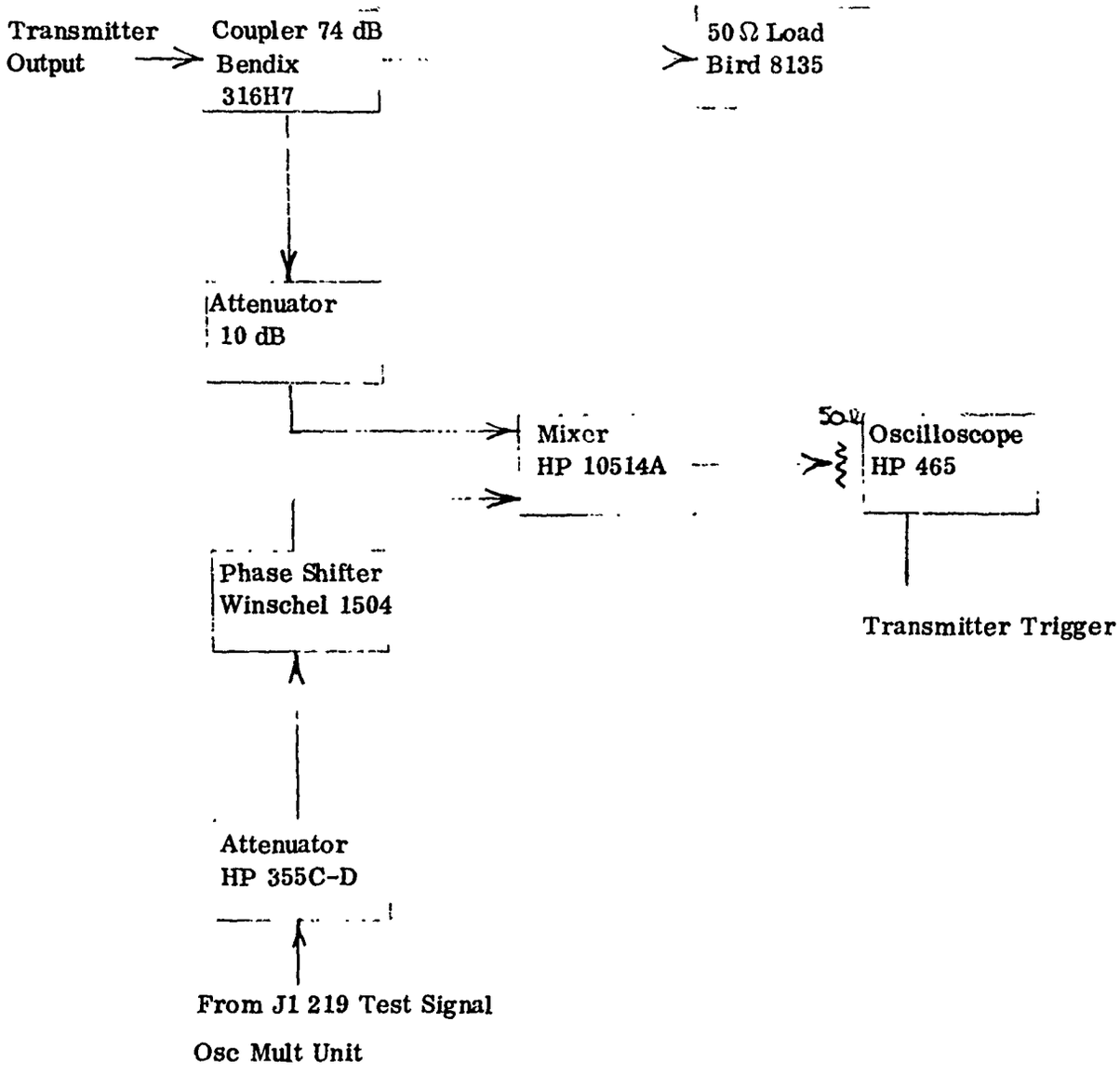


Figure (2) - Relative Phase Measurements of Transmitter Outputs.

Step 5. Turn transmitter on as in A2 a.2

Step 6. Phase measurement calibration

a. Adjust attenuator from J1 test signal for 0 dBM at input to mixer.

b. Adjust phase shifter for maximum pulse amplification on scope. Note position of peak pulse.

c. Adjust phase shifter for 0 volts at position of the peak pulse and record setting of phase shifter.

d. Repeat for each transmitter output using the same cable length from output connector to coupler (74 dB) and coupler to load (BIRD 8135)
NOTE: Unused transmitter outputs to be terminated into 50 ohms load (BIRD 8135).

b. Expected Results

1. Power output 25 KW min

2. Phase between outputs $\pm 5^{o}$ max

3. Pulse width 125 ns max at 3 dB

B. Processor

1. Verify Operation of Analog-to-Digital Converters (ADC's):
The ADC's will be checked for offset bias correction and general operation using the processor test target simulate function in conjunction with the scan converter and display. NOTE: For identification and location of processor and scan converter controls refer to METRRA Maintenance Manual.

a. Procedure

Step 1. Interconnect processor, processor control panel, scan converter (S/C), S/C control panel and monitor display with their respective cabling as per METRRA Maintenance Manual. Connect 28 V primary power.

Step 2. Provide a 20 KHz pulse source to the system PRF input J110 (T^2L into 50)

Step 3. Turn on processor in system mode and allow 5 min warm up

Step 4. Observe Fund and HARM Bit Level Indicators on processor control panel (see Results 1).

Step 5. Turn on S/C and display in Operate mode (allow 5 min warm up)

Step 6. Place processor in Test, Target Simulate mode.

Step 7. Adjust Limit and Round/off switches (processor control panel) and Gain and Offset controls (S/C control panel) for optimum display. (See Results 2).

b. Results

1. All bit indicator lights should be extinguished (with the exception of occasional lighting of lower order bits).

2. A display of twelve columns of dots equally spaced vertically should be on the monitor display.

2. Verify Range Data Fill-in:

The processor range data fill-in function was altered such that targets which are saturated in the processor can not appear as three separate targets in range on the monitor display due to data fill-in. Since data fill-in is common to I & Q channels of both the Harmonic and Fundamental, operation may be demonstrated by providing a digital target input continuous in azimuth into any channel.

a. Procedure

Step 1. Remove BRDS P2, 4, 6 of ADC card rack.

Step 2. Connect pulse generator as per Figure 3 (provides continuous target in range).

Step 3. Turn on processor and S/C in Test mode.

Step 4. Adjust HARM Limit and Round-off switch to below bit level indicated by Harm Bit Level Indicator. This provides a saturated signal.

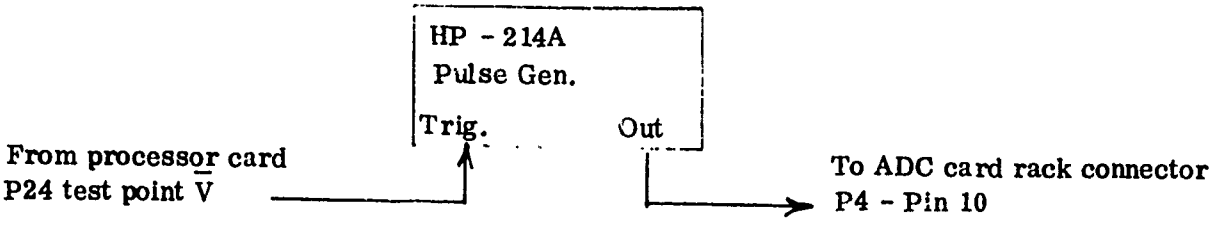


Figure (3) - Range Data Fill-in.

Step 5. Adjust pulse generator for ~200 ns pulse or narrow stripe on display.

Step 6. Adjust the HARM Offset and Gain controls (S/C control panel) such that the center of the stripe, in range, does not saturate the display and has maximum dynamic range from the center to the edges of the stripe.

b. Expected Results

1. The displayed stripe should be monitonically decreasing in intensity at the edge of the stripe.

3. Verify Calibration of Near Range Dial and Near Range Sample

a. Procedure

Step 1. Extend processor card P24 and connect counter as in Figure 4.

Step 2. Turn on processor and set Near Range to 1 KM (See results.)

b. Expected Results

Range Setting	Time
1 KM	6.6 μs ± .1μs
2 KM	13.3 μs
3 KM	20.0 μs

4. Verify that Harmonic and Fundamental Data do not Overlay at Near and Far Range

a. Procedure

Step 1. Provide 20 KHz pulses at processor input J-110.

Step 2. Remove card P6 of ADC rack and jumper pins 4, 6, 8, 10, 12, 14, 16 and 18 of P6 rack connector to logic "1" (provides max input fundamental I & Q inputs).

Step 3. Turn processor and S/C on in System mode.

Step 4. Adjust processor and S/C controls for saturated fundamental display

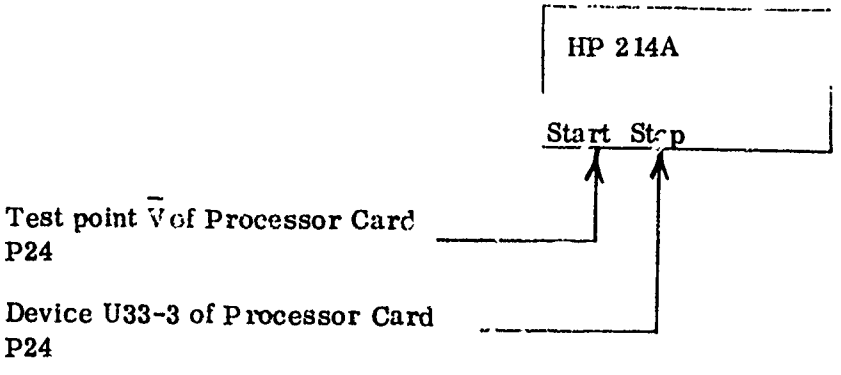


Figure (4) - Near Range Calibration.

Step 5. Select Harmonic Only (see results 1).

Step 6. Turn processor off, remove jumper and replace card P6 and remove cards P2 and P4 from ADC card rack and install jumpers. (Provides max Harmonic as in Step 2 input.)

Step 7. Repeat steps 3 and 4 for Harm.

Step 8. Select Fundamental Only (see results 2).

b. Expected Results

Step 1. In steps 5 and 8 display should be a uniform dark gray indicating no signal. A white stripe may be seen at near range (1st range cell) as a result of residues in the range data fill-in circuits.

5. Verify Square Aspect Ratio Display:

Azimuth data resampling has been added to the scan converter to provide an equal range and azimuthdimension on the display, independent of azimuth resolution.

a. Procedure

Step 1. Turn on the processor and S/C with the processor in the Test Target Simulate mode, Near Range Switch = 1 KM, and S/C in System Mode.

Step 2. Adjust processor and S/C controls for uniform display of twelve columns of targets which are uniformly spaced in range.

Step 3. Place S/C in Hold mode and measure height of screen and vertical distance between targets. Record.

b. Expected Results

Targets are generated every 20 Harmonic elements (W_H). The distance between targets is then 20 W_H where

$W_H = \sqrt{R\lambda_H}$ and $\lambda_H = .46$ M (Harmonic Wavelergth)

The display distance between targets is:

$$\frac{\text{Target Separation in Meters}}{\text{Az Full Scale in Meters}} \times H_D$$

where H_D = height of diaplay

Az Full Scale in Meters = .75 Range Swath = 1085

The following are target ground separation and display separation at various ranges on a 5 1/2 inc vertical monitor.

Range in KM	Target Separation in Meters	Display Separation in inch for H_D = 5 1/2 in.
1	430	2.18 ±5%
2	586	2.96 ±5%
3	878	4.45 ±5%

EQUIPMENT LIST

1. 4 - 505L term. BIRD Model 8135
2. 1 - Directional coupler Bendix Mod 316H7
3. 1 - Crystal detector H.P. Mod 423A
4. 1 - Precision phase shifter Weinschel Engineering Mod 1504
5. 1 - Attenuator H.P. Mod 355C
6. 1 - Attenuator H.P. Mod 355D
7. 1 - Mixer H.P. 10514A
8. Oscilloscope Techtronix 465
9. Function Gen. H.P. 3310B
10. Counter H.P. 5345A
11. Pulse generator H.P. 214A